Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend claims 14, 16, 19, 24, 26, and 27 as follows:

Claims 1-13 (previously canceled).

14. (currently amended): An array processor comprising:

a physical MxN array organization of at least two processing elements (PEs) and a sequence ~~control~~ processor (SP), each of the at least two PEs having a set of PE register files and the SP ~~control processor~~ having a set of SP ~~control~~ register files, the ~~control processor~~SP and at least one PE combined to form a combined processor, the combined processor having substantially similar access to the set of ~~control~~ SP register files and to the set of PE register files of the at least one PE that was combined to form the combined processor; and

a processor state register storing a context ~~status~~ switch bit (CSB), the CSB having a first state and a second state, the ~~control processor~~SP and each PE operating to detect the state of the CSB,

the combined processor upon detection of the first state of the CSB operating in a first operating context stored ~~on~~ in the set of ~~control~~ SP register files, the first operating context adapted for processing a first software task where the first software task is written for an MxN operating configuration which matches the physical MxN array organization including the at

least one PE of the combined processor, where M represents the number of rows of PEs and N represents the number of columns of PEs,

the combined processor upon detection of the second state of the CSB operating in a second operating context stored ~~on~~ in the set of PE register files of the combined processor, the second operating context adapted for a second software task where the second software task is written for an OxP operating configuration of the physical MxN array organization where O is the number of rows of PEs and P is the number of columns of PEs, the OxP operating configuration not matching the physical MxN array organization as O+P<M+N.

15. (previously canceled)

16. (currently amended): The array processor of claim 14 further comprising:

an eventpoint mechanism to trigger a context switch from the OxP operating configuration to the MxN operating configuration by storing the data contents of the set of PE register files of the combined processor and the PEs in the background while the first software task uses the set of ~~control~~ SP register files in the foreground, whereby the OxP operating configuration is saved.

17. (previously presented): The array processor of claim 14 further comprising:

an eventpoint mechanism to trigger a context switch from the MxN operating configuration to the OxP operating configuration by loading the set of PE register files of the combined processor and the PEs in the background with the data contents associated with the OxP operating configuration and after all of the data contents have been loaded, the combined processor switches to the second software task.

18. (previously presented): The array processor of claim 14 wherein each processing element of the at least two processing elements has a physical identifier and a virtual identifier, wherein during the processing of the first software task, instructions are operable in each processing element according to its physical identifier, wherein during the processing of the second software task, instructions are operable in each processing element according to its virtual identifier taking into account the at least one PE that was combined to form the combined processor.

19. (currently amended): A method for providing reconfiguration of a first array processor having a physical MxN array organization to emulate operation of a second array processor having a physical OxP array organization where M and O represent the number of rows of processing elements (PEs) and N and P represent the number of columns of PEs, the method comprising:

providing the first array processor having at least two PEs arranged in the physical MxN array organization and having a sequence processor (SP), each of the at least two PEs having a set of PE register files and the SP having a set of ~~control~~ SP register files;

combining the SP and at least one PE to form a combined processor, ~~wherein~~ the combined processor having substantially similar access to the set of ~~control~~ SP register files and to the set of ~~compute~~ PE register files of the at least one PE that was combined to form the combined processor;

storing a context ~~status~~ switch bit (CSB), the CSB having a first state and a second state;

detecting the state of the CSB;

upon detection of the first state, operating in a first operating context stored ~~on~~ in the set of ~~control~~ SP register files, the first operating context adapted for processing a first software task, wherein the first software task is written for an MxN operating configuration which matches the physical MxN array organization including the at least one PE of the combined processor; and

upon detection of the second state, operating in a second operating context stored ~~on~~ in the set of PE register files of the combined processor, the second operating context adapted for processing a second software task, wherein the second software task is written for an OxP operating configuration on an OxP subset of the physical MxN array organization, where either M≠O or N≠P.

20. (previously presented): The method of claim 19 wherein the operating in the second operating context step further comprises:

setting the CSB to the first state; and

returning the processing to the first operating context.

21. (previously presented): The method of claim 19 wherein the physical MxN array organization comprises a 1x1 layout and the emulated physical OxP array organization comprises a 1x0 layout, wherein the 1x0 layout defines the sequence processor (SP) executing sequential instructions.

22. (previously presented): The method of claim 19 wherein the physical MxN array organization comprises a 1x2 layout and the emulated physical OxP array organization comprises a 1x1 layout.

23. (previously presented): The method of claim 19 wherein the physical MxN array organization comprises a 1x5 layout and the emulated physical OxP array organization comprises a 2x2 layout.

24. (currently amended): An apparatus for providing efficient sharing of programming resources in a merged very long instruction word (VLIW) sequence processor (SP) and VLIW processor element (PE) processor, the merged VLIW SP/PE processor operating to configure an array processor to operate in an MxN operating configuration or in an OxP operating configuration, where M and O are the number of rows of processing elements and N and P are the number of columns of processing elements, and where O+P<M+N, the apparatus comprising:

an SP resource file having a first set of registers;

a PE resource file having a second set of registers;

an input for receiving a VLIW presented for execution, the VLIW having at least two instructions, each instruction encoded with a different setting of an SP/PE-bit, wherein the state of the SP/PE-bit determines whether an instruction is an SP instruction or a PE instruction; and

a processor state register storing a context ~~select~~ switch bit (CSB), the merged VLIW SP/PE processor reading the values of the CSB and the SP/PE-bit of each instruction, the value of the CSB selecting the MxN operating configuration or the OxP operating configuration when processing ~~the~~ each instruction, the MxN operating configuration adapted for accessing at least one register from the first set of registers when processing an SP instruction as one of the at least two instructions and for accessing at least one register from the second set of registers when

processing ~~an~~ a PE instruction as the other instruction of the at least two instructions based on the value of the SP/PE-bit.

25. (previously presented): The apparatus of claim 24 wherein the OxP operating configuration is adapted for accessing at least one register from the second set of registers when processing an SP instruction and accessing at least one register from the second set of registers when processing a PE instruction based on the value of the SP/PE-bit.

26. (currently amended): The apparatus of claim 24 wherein the SP resource file is an SP register file, an SP address register file, or ~~a~~ an SP machine state register file.

27. (currently amended): The apparatus of claim 24 wherein the PE resource file is a PE register file, PE address register file, or a PE machine state register ~~files~~file.

28. (previously presented): The apparatus of claim 24 further comprising:

at least two execution units associated with the at least two instructions in the VLIW; and

a plurality of multiplexers connected to the SP and PE resource files for selecting resource files from which the at least two execution units read data and to which the at least two execution units write data, a portion of the plurality of multiplexers associated with an execution unit controlled by a logical combination of the SP/PE bit and the CSB.

29. (previously presented): The apparatus of claim 24 wherein the VLIW SP processor and VLIW PE processor are indirect VLIW processors.